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No. of Printed Pages: 2

SARDAR PATEL UNIVERSITY

M. Sc. I. T. (Integrated) Examination, 2nd Semester

Wednesday, 13th April, 2016

PS02EIIT01: Digital Electronics

Time: 10:30 AM to 12:30 PM **Total Marks: 70**

Note: Answer of all the questions (including Multiple Choice Questions) should be written in the provided answer book only

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Q:1 Give answers of following Multiple Choice Questions [10]

[01] De Morgan's first theorem says that a NOR gate is equivalent to a _____.

(A) bubbled OR (B) bubbled NOR
(C) bubbled AND (D) AND bubbled

[02] A combinational circuit that performs the arithmetic addition of two bits is called _____.

(A) Full Adder (B) Half Adder
(C) Binary Adder (D) Decoder

[03] Half adder consists of. _____ and _____ Gates

(A) XNOR, AND (B) XNOR, OR
(C) XOR, AND (D) XOR, OR

[04] A 4 – to – 1 line multiplexer requires _____ data select line.

(A) 1 (B) 2
(C) 3 (D) 4

[05] Which device has many input and one output?

(A) Flip – Flop (B) Multiplexer
(C) De-Multiplexer (D) Counter

[06] In Comparator, _____ gate is use for comparing bits in word.

(A) XOR (B) AND
(C) NOR (D) XNOR

[07] In k-map, quad eliminates _____ variable.

(A) One (B) Two
(C) Three (D) Four

[08] The 4-variable Karnaugh Map (K-Map) has _____ rows and _____ columns

(A) 2, 2 (B) 4, 4
(C) 4, 2 (D) 2, 4

[09] Which of the following is Universal flip-flop?

(A) JK flip-flop (B) RS flip-flop
(C) Master slave flip-flop (D) D flip-flop

[10] Shift register move the stored bits _____ or _____.

(A) Left or right (B) Left or left
(C) Right or right (D) Up or down

Q:2 Answer the following short questions (any Ten) **[20]**

[01] Explain De Morgan first theorem.
[02] Describe binary adder in short.
[03] Draw the circuit of encoder.
[04] Draw the circuit of Seven Segment Decoder.
[05] Draw the circuit of 4x1 line multiplexer.
[06] Draw the circuit of 4x1 line de-multiplexer.
[07] Define Karnaugh map in detail.
[08] Explain K-Map for 2 variable with example.
[09] Describe octet in k-map
[10] Draw circuit diagram of D flip-flop
[11] Define flip-flop.
[12] Explain shift left register in brief.

Q:3 [A] Explain half adder in detail. **[05]**

[B] Explain 8x3 line encoder in detail. **[05]**

OR

Q:3 [C] Explain binary adder-subtractor in detail. **[05]**

[D] Explain 3x8 line decoder in detail. **[05]**

Q:4 [A] Explain 8x1 line multiplexer with circuit in detail. **[05]**

[B] Write a short note on Comparator with circuit diagram. **[05]**

OR

Q:4 [C] Explain 8x1 line de-multiplexer with circuit in detail. **[05]**

[D] Write a short note on Nibble Multiplexer with circuit. **[05]**

Q:5 [A] What is k-map? Explain pair and quad with example. **[05]**

[B] Simplify this using k-map $F(A,B,C,D)=\sum(1,3,5,6,8,11,15)$ **[05]**

OR

Q:5 [C] Write a short note on Don't Care Condition. **[05]**

[D] Simplify this using k-map $F(A,B,C,D)=\sum(1,2,5,6,8,12,14)$ **[05]**

Q:6 [A] Explain RS flip-flop in detail. **[05]**

[B] Explain controlled buffer register in detail. **[05]**

OR

Q:6 [C] Explain JK flip-flop in detail. **[05]**

[D] Explain ring counters in detail. **[05]**