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[521]

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**SARDAR PATEL UNIVERSITY**
**M.Sc. (Electronics & Communication) (Semester-II) Examination**
**Day & Date: Saturday, 25-04-2015**
**Time: 2:30 p.m. to 5:30 p.m.**
**Subject: Digital Electronics**
**Paper No. PS02CELC03**

**Instructions:** **Marks: 70**
**--Figures to the right indicate marks.**

**Q-1** **Choose the correct answer.** **[8]**

1. How many binary numbers are created with 8-bits?
   a)512 b) 256 c) 128 d) 64
2. In MSI the number of gate circuit per chip is _____.
   a)<6 b)<12 c)<100 d)<1000
3. An n variable K-map have _____.
   a) $2^n$ cells b) $n^2$ cells c) $n^n$ cells d) $n^{2n}$ cells
4. An Eight square eliminate _____ variable.
   a)3 b)4 c)5 d)6
5. A_____ is a logic circuit that compares the magnitude of 2-bit binary number.
   a)1-bit magnitude comparator b)2-bit magnitude comparator
   c)3-bit magnitude comparator d)4-bit magnitude comparator
6. A Johnson counter has a initial state Q1=1, Q2=0, Q3=0, Q4=0, What will be the state of Q1, Q2, Q3, Q4 output of the counter after the $7^{th}$ clock pulses.
   a) 1110 b) 1100 c) 0000 d) 0001
7. In RS flip-flop R=S=1, the state $Q_{n+1}$ of the flip flop after the clock pulse will be _____.
   a) reset b) set c) indeterminate d) no change
8. An 8-bit synchronous counter uses flip-flop with propagation delay time of 100 ns each. The maximum possibilities time required for change of state will be_____.
   a)100 ns b)75ns c)50ns d)25ns

**Q-2** **Answer in short. (Any SEVEN)** **[14]**

1. How BCD addition is performed?
2. What is meant by weighted and Non-weighted codes?
3. State De-Morgan first and second theorem.
4. What is K-map? What are the advantages and disadvantages of it's?
5. Which gates are called universal building blocks? Why?
6. Explain 1-bit magnitude comparator.
7. Explain RS flip-flop.
8. What is shift register? What is the basic difference between shift register and counter?
9. Give the difference between Serial and Parallel counter.

(P.T.O)

**Q-3 (a)** Perform the following. **(6)**
(I) Convert $(105.15)_{10}$ to binary.
(II) Convert $(4057.06)_8$ to decimal.
(III) Convert $(110101.101010)_2$ to octal.

**(b)** With necessary circuit diagram explain Johnson counter. **(6)**

**OR**

**(b)** With necessary circuit diagram, truth table and waveforms explain MOD-8 synchronous counter. **(6)**

**Q-4 (a)** Reduce the expression F=∑M (0, 2, 3, 4, 5, 6) by SOP and implement in to NAND logic. **(6)**

**(b)** Perform the following. **(6)**
(I) Subtract 14 from 46 using 8-bit 2's complement method.
(II) Perform the XS-3 addition of 37and 28.
(III) Find the 10's Complement of the 4069.

**OR**

**(b)** Reduce the expression F=∑m (0,1,2,5,8,9,10) by SOP. Also count how many inputs required by the converting in to simple logic circuit . **(6)**

**Q-5 (a)** Reduce the following Boolean expression: $\overline{\overline{A\bar{B} + ABC + A(B + A\bar{B})}}$ **(6)**

**(b)** Perform the following. **(6)**
(I) Subtract 15 from 38 using BCD subtraction method.
(II) Subtract 27 from 57 using XS-3 code.
(III) Convert gray 111001 to binary.

**OR**

**(b)** Explain 2-bit magnitude comparator in detail with necessary diagram. **(6)**

**Q-6 (a)** Explain edge triggered D flip-flop in detail. **(6)**

**(b)** What is PLA? Show how PLA circuit can be programmed to implement the 3-bit binary to Gray converter. **(6)**

**OR**

**(b)** Give detail account of Master slave JK flip-flop. **(6)**

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